What is claimed is:

1. An imprinting apparatus comprising:

a semiconductor substrate polished in a [110] direction, the semiconductor substrate having a (110) horizontal planar surface and vertical sidewalls of a wet chemical etched trench, the trench vertical sidewalls are aligned with (111) vertical lattice planes of the semiconductor substrate, the semiconductor substrate comprising a plurality of vertical structures between the trench vertical sidewalls, the trench vertical sidewalls and the plurality of vertical structures being spaced apart from each other to form a mold that provides a pattern for imprinting.

2. The imprinting apparatus of Claim 1, wherein the semiconductor substrate is wet chemical etched along the (111) vertical lattice planes using an etching solution that etches the (111) vertical lattice plane much slower than a (110) horizontal lattice plane to form the trench.

3. The imprinting apparatus of Claim 1, wherein the semiconductor substrate is silicon, the etching solution being selected from potassium hydroxide, ethylene diamine pyrocatechcol and tetramethylammonium hydroxide.

4. The imprinting apparatus of Claim 1, wherein the semiconductor substrate is a material selected from one of a Group IV element, Group III-V elements, and Group II-VI elements, the semiconductor substrate being wet chemical etched along the (111) vertical lattice planes.

5. The imprinting apparatus of Claim 1, wherein the semiconductor substrate is wet chemical etched along the (111) vertical lattice planes such that the trench sidewalls have smooth surfaces relative to trench sidewalls that are dry chemical etched.

6. The imprinting apparatus of Claim 1, wherein the semiconductor substrate is wet chemical etched along the (111) vertical lattice planes such that the trench

sidewalls have reduced crystal structure damage relative to trench sidewalls that are dry chemical etched.

7. The imprinting apparatus of Claim 1, wherein the semiconductor substrate is a silicon layer of a silicon-on-insulator wafer polished in the [110] direction.

8. The imprinting apparatus of Claim 1, wherein the plurality of vertical structures are nano-scale spaced using a deposited nano-scale thick layer of a first material alternating with a deposited nano-scale thick layer of a second material in the trench, the first material being different from the semiconductor substrate and the second material, the first material being adjacent the trench sidewall, the second material being adjacent the first material, the first material being selectively removed from between the trench sidewalls and vertically extending portions of the second material layers.

9. The imprinting apparatus of Claim 8, wherein the semiconductor substrate is silicon, the first material being selected from silicon dioxide, silicon nitride and germanium, the second material being selected from silicon, silicon dioxide, silicon nitride and germanium, and wherein the first material is selectively removed from between the trench sidewalls and the vertically extending portions with an etchant that preferentially removes the first material instead of the silicon substrate and the second material.

10. The imprinting apparatus of Claim 1, wherein the plurality of vertical structures are walls of the semiconductor substrate separating adjacent parallel trenches, the parallel trenches being etched in the semiconductor substrate between the trench vertical sidewalls.

11. The imprinting apparatus of Claim 1, wherein the plurality of vertical structures are walls separating adjacent parallel trenches, the walls being aligned with different ones of (111) vertical lattice planes of the semiconductor substrate and wet chemical etched along with the trench vertical sidewalls.

12. The imprinting apparatus of Claim 1, wherein the mold pattern has a vertical structure spacing in one or both of a nanometer range and a micrometer range.

13. A nano-imprinting apparatus comprising:

a semiconductor substrate having a horizontal (110) planar surface and a plurality of (111) vertical lattice planes intersecting the (110) planar surface;

sidewalls of a trench etched in the semiconductor substrate along spaced apart (111) vertical lattice planes of the plurality using wet chemical etching, such that the trench sidewalls are (111) vertical planes; and

a plurality of nano-scale spaced vertical structures disposed in the trench spaced from the vertical sidewalls, a vertical structure having opposing sides and an end, a side of the vertical structure facing one or both of a side of an adjacent vertical structure and a trench sidewall, the end having a horizontal surface coplanar with the (110) planar surface of the semiconductor substrate,

wherein the plurality of vertical structures between the trench sidewalls provides a nano-scale pattern for nano-imprinting.

14. The nano-imprinting apparatus of Claim 13, wherein the trench is wet chemical etched along the (111) vertical lattice planes using an etching solution that etches the (111) vertical lattice plane much slower than the (110) planar surface.

15. The nano-imprinting apparatus of Claim 14, wherein the semiconductor substrate is silicon, the etching solution being selected from potassium hydroxide, ethylene diamine pyrocatechcol and tetramethylammonium hydroxide.

16. The nano-imprinting apparatus of Claim 13, wherein the semiconductor substrate is a material selected from one of an element from Group IV, elements from Group III-V, and elements from Group II-VI.

17. The nano-imprinting apparatus of Claim 13, wherein the vertical sidewalls of the trench have one or both of smooth sidewalls and reduced crystal structure damage relative to trench sidewalls that are dry chemical etched.

18. The nano-imprinting apparatus of Claim 13, wherein the semiconductor substrate is a silicon layer of a silicon-on-insulator wafer polished in a [110] direction.

19. The nano-imprinting apparatus of Claim 13, wherein the vertical structures comprise a material selected from silicon, silicon dioxide, silicon nitride and germanium deposited in the trench by a chemical vapor deposition.

20. The nano-imprinting apparatus of Claim 13, wherein the vertical structures are nano-scale spaced using deposited nano-scale thick layers of a first material alternating with deposited nano-scale thick layers of a second material in the trench, the first material being different from the semiconductor substrate and the second material, the first material being adjacent the trench sidewall, the second material being adjacent the first material, the first material being selectively removed from between the trench sidewalls and vertically extending portions of the second material layers in the trench.

21. The nano-imprinting apparatus of Claim 20, wherein the semiconductor substrate is silicon, the first material being selected from silicon dioxide, silicon nitride and germanium, the second material being selected from silicon, silicon dioxide, silicon nitride and germanium.

22. The nano-imprinting apparatus of Claim 13, wherein the plurality of vertical structures are walls of the semiconductor substrate separating adjacent parallel trenches, the parallel trenches being etched in the semiconductor substrate between the trench sidewalls.

23. The nano-imprinting apparatus of Claim 22, wherein the adjacent parallel trenches are wet chemical etched along (111) vertical lattice planes of the semiconductor substrate along with the trench.

24. The nano-imprinting apparatus of Claim 13, wherein the nano-scale pattern has one or both of a vertical structure spacing that ranges from about 5 nm to

about 100 μm and a vertical structure pitch that ranges from about 10 nm to about 200 μm.

25. A method of fabricating an imprinting apparatus comprising:

wet etching a semiconductor wafer polished in a [110] direction, the semiconductor wafer having a (110) horizontal surface, a portion of the (110) horizontal surface being exposed, the exposed portion being aligned between (111) vertical lattice planes of the semiconductor wafer, the semiconductor wafer being wet etched with a chemical etching solution that etches the (111) vertical lattice planes slower than a (110) horizontal lattice plane to form a trench having spaced apart (111) vertical sidewalls in the semiconductor wafer; and

forming a mold with a pattern for imprinting,

wherein the vertical sidewalls have smooth surfaces relative to vertical sidewalls etched with a dry chemical etching process.

26. The method of fabricating of Claim 25, wherein the etched semiconductor wafer has reduced crystal structure damage relative to a semiconductor wafer etched with a dry chemical etching process.

27. The method of fabricating of Claim 25, further comprising:

providing the semiconductor wafer polished in a [110] direction, the (110) horizontal surface being planar or aligned with the (110) horizontal lattice plane; and

masking the (110) horizontal surface with an etch mask, the etch mask being patterned such that mask pattern edges are aligned along (111) vertical lattice planes that intersect with the (110) horizontal plane or surface to produce the exposed portion.

28. The method of fabricating of Claim 25, wherein the semiconductor wafer is a silicon layer of a silicon-on-insulator wafer polished in the [110] direction.

29. The method of fabricating of Claim 25, wherein the semiconductor wafer is selected from a material selected from one of an element from Group IV, elements from Group III-V, and elements from Group II-VI.

30. The method of fabricating of Claim 25, further comprising:

depositing alternating layers of a first material and a second material in the trench between the spaced apart (111) vertical sidewalls, the first material being deposited adjacent to the trench sidewalls in a first layer and deposited adjacent to the second material in subsequent layers; and

selectively removing the first material from between the trench sidewalls and vertically extending portions of the second material layers, such that spaced apart vertical walls of the second material extend parallel between the (111) vertical sidewalls, the vertical walls having ends coplanar with the (110) horizontal surface of the semiconductor wafer.

31. The method of fabricating of Claim 30, wherein the first material is different from the semiconductor substrate and the second material, the first material being selected from silicon dioxide, silicon nitride and germanium, the second material being selected from silicon, silicon dioxide, silicon nitride and germanium, and wherein the first material is selectively removed using an etchant that is more selective for the first material than the trench sidewalls of the substrate and the second material.

32. The method of fabricating of Claim 30, further comprising:

removing any of the alternating layers from the (110) horizontal surface before selective removal.

33. The method of fabricating of Claim 32, wherein the alternating layers are removed from the (110) horizontal surface using one or both of chemical polishing and mechanical polishing.

34. The method of fabricating of Claim 25, wherein the mold pattern has a vertical sidewall spacing in one or both of a nanometer range and a micrometer range.

35. A method of fabricating a nano-imprinting mold comprising:

masking a (110) horizontal planar surface of a semiconductor wafer polished in the [110] direction with an etch mask aligned with a (111) vertical lattice plane in the semiconductor wafer;

wet etching the semiconductor wafer along the (111) vertical lattice plane, such that a trench is formed having vertical sidewalls and a relatively horizontal bottom, the vertical sidewalls having the (111) vertical lattice planes of the semiconductor wafer;

depositing alternating layers of a first material and a second material on the wet-etched semiconductor wafer, such that the alternating layers cover the sidewalls and the bottom of the trench; and

selectively removing the first material from between the trench sidewalls and vertically extending portions of the second material layers in the trench, such that nano-scale spaced vertical walls of the second material extend parallel between the vertical sidewalls of the trench, the spaced apart walls and the vertical sidewalls forming a nano-scale mold for nano-imprinting.

36. The method of fabricating of Claim 35, wherein the alternating layers are further deposited on the (110) horizontal planar surface of the semiconductor wafer, and wherein the method further comprises removing the alternating layers from the (110) horizontal planar surface before selectively removing.

37. The method of fabricating of Claim 36, wherein the alternating layers are removed from the (110) horizontal planar surface using mechanical polishing, the mechanical polishing making the ends of the walls coplanar with the exposed (110) horizontal planar surface.

38. The method of fabricating of Claim 35, wherein wet etching comprises using an etching solution that etches the (111) vertical lattice planes slower than (110) horizontal lattice planes of the semiconductor wafer.

39. The method of fabricating of Claim 35, wherein wet etching provides one or both of smooth sidewall surfaces and reduced crystal damage to the semiconductor wafer relative to a semiconductor wafer etched with a dry chemical etchant.

40. The method of fabricating of Claim 35, wherein the semiconductor wafer is a silicon layer of a silicon-on-insulator wafer polished in the [110] direction.

41. The method of fabricating of Claim 35, wherein the first material is different from the semiconductor wafer and the second material, the first material and the second material being independently selected from silicon, silicon dioxide, silicon nitride and germanium, the semiconductor wafer being a material selected from one of an element from Group IV, elements from Group III-V, and elements from Group II-VI.

42. The method of fabricating of Claim 35, wherein the semiconductor wafer is a material selected from one of a Group IV element, Group III-V elements, and Group II-VI elements.